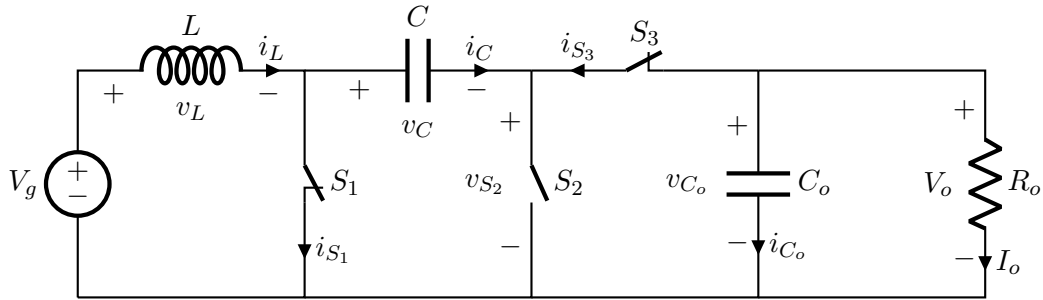**Q1:** $for\ 0 \leq t < DT_s$

Figure 1: Circuit when S1, S3 are turned -ON and S2 is turned -OFF
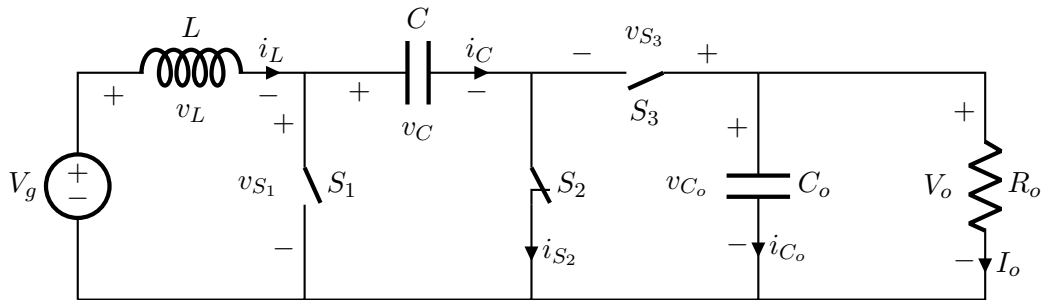
Q2: $for\ DT_s \leq t < T_s$

Figure 2: Circuit when S1, S3 are turned -OFF and S2 is turned -ON

Q3

Three main assumptions which can be used to simplify the analysis of a switching circuit.

1. **Steady state operation**: At each cycle the operation of the circuit is identical.

2. **Small ripple approximation**: Therefore $v_o(t) = V_o + v_{ripple}(t)$ is simplified into $v_o(t) = V_o$ using the fact that $|v_{ripple}(t)| \ll V_o$ which is caused by non-ideal filtering.

3. **Sufficiently large capacitance**: Throughout the operation capacitors will maintain constant voltages.

Q4

Consider the operation of the circuit for $0 \leq t < DT_s$

* Associated Voltages

Since the S_1 switch is ON, positive and negative terminals of the source are directly connected to the positive and negative terminals of the inductor(L) respectively.

$$v_L = V_g \tag{1}$$

Since the S_3 switch is also ON, positive terminal of the capacitor C is connected to the negative terminals of the capacitor C_o and resistor R_o. While negative terminal of the capacitor C is connected to the positive terminals of the capacitor C_o and resistor R_o. In addition to that as C_o and R_o are in parallel $v_{C_o} = V_o$.

Using the Kirchhoff voltage Low to that loop,

$$v_C + V_o = 0 \qquad \qquad \therefore v_C = -V_o$$

Consider the operation of the circuit for $DT_s \leq t < T_s$

* Associated Voltages

Using the Kirchhoff voltage Low,
$$V_g = v_L + v_C$$

Since we assume sufficiently large capacitance, change in v_C is negligible from the previous state of the circuit.
$$\therefore V_g = v_L + (-V_o)$$

Rearranging,
$$v_L = V_g + V_o \tag{2}$$

From equations (1) and (2),
$$v_L = \begin{cases} V_g & for\ 0 \leq t < DT_s \\ V_g + V_o & for\ DT_s \leq t < T_s \end{cases}$$

As we are analyzing a switching circuit which has the ability to invert and step-up its supply voltage, $|V_g| < |V_o|\ and\ V_o < 0$. Which implies $V_g + V_o < 0$.

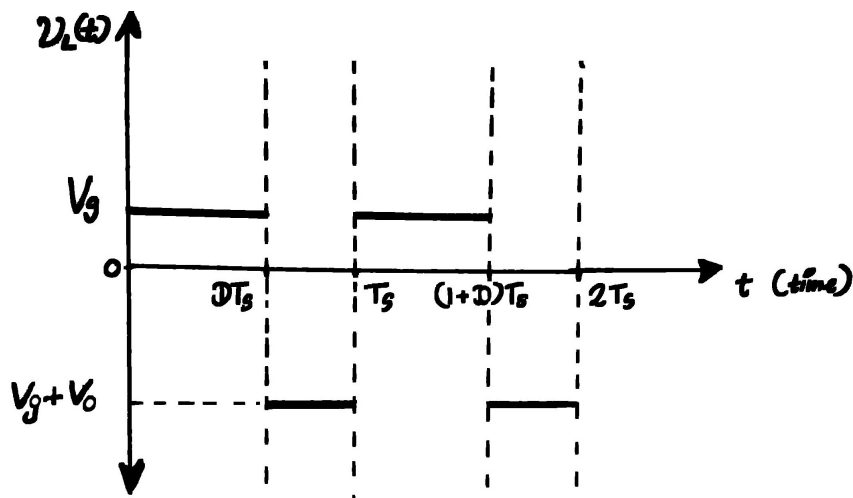

Figure 3: Inductor voltage $v_L(t)$

Since voltage drop across an inductor is related to the current through it according the following differential equation, graph of the i_L can be directly deduced from the graph of the v_L.

$$v_L = L.\frac{d\,i_L}{dt}$$
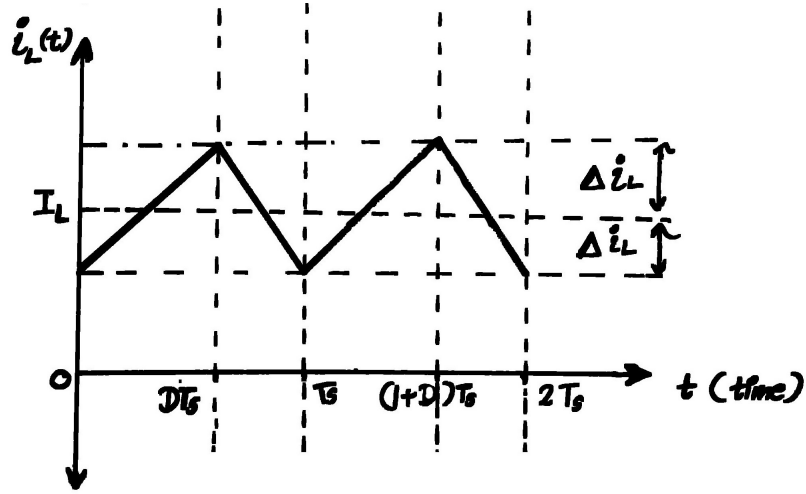

Figure 4: Inductor current $i_L(t)$

In the above figure I_L denotes the average inductor current.

Q5

Using inductor volt-second balance,

$$< V_L(t) > = 0 = \frac{1}{T_s}.\int_0^{T_s} V_L(t)\ dt$$

$$= \int_0^{DT_s} V_L(t)\ dt + \int_{DT_s}^{T_s} V_L(t)\ dt$$

$$= \int_0^{DT_s} V_g\ dt + \int_{DT_s}^{T_s} V_g + V_o\ dt$$

$$= V_g.DT_s + (V_g + V_o).(T_s - DT_s)$$

$$= V_g.D + (V_g + V_o).(1 - D)$$

$$= V_g + V_o.(1 - D)$$

$$\therefore V_o = -\frac{V_g}{1 - D}$$

Q6

S1

- ON Current(i_{S_1})

  As described below in the part "**S3**", i_{S_3} is positive in the marked direction. Therefore according to the Kirchhoff Current Low, $i_C + i_{S_3} = 0$ and it implies i_C is negative in the marked direction(actual direction is the opposite of the marked direction). As v_L is positive i_L is positive in the marked direction. Because of these reasons, according to the K.C.L, $i_{S_1} = i_L + (-i_C)$ and it is positive in the marked direction in Fig.1.

- Blocking Voltage(v_{S_1})

  From Fig.2, positive and negative terminals of the switch are connected to the positive and negative terminals of the capacitor C. Therefore $v_{S_1} = v_C$. From the calculations of the Question 04, $v_C = -V_o$ and V_o is negative. Therefore v_{S_1} is positive.

S2

- ON Current(i_{S_2})

  When considering the loop consist of the Source,inductor, capacitor(C) and the switch S_2 in Fig.2, it is obvious that i_{S_2} is positive in the given direction.

- Blocking Voltage(v_{S_2})

  From Fig.1, $v_{S_2} = v_{C_o} = V_o$. Since V_o is negative, v_{S_2} is also negative.

S3

- ON Current(i_{S_3})

  Since V_o and v_{C_o} are negative in the marked direction, their currents are also in the direction opposite to the marked direction. Therefore according to the Kirchhoff Current Low, $i_{S_3} = -(i_{C_o} + I_o)$. Which results i_{S_3} to be positive in the marked direction in Fig.1.

- Blocking Voltage(v_{S_3})

  From Fig.2, $v_{S_3} = V_o$ as positive and negative terminals of the switch are connected to the positive and negative terminals of the R_o respectively. Since V_o is negative, v_{S_3} is also negative.

Switch	ON-current	Blocking Voltage	Suitable Semiconductor Device
S1	$i_{S_1} > 0$	$v_{S_1} > 0$	FET
S2	$i_{S_2} > 0$	$v_{S_2} < 0$	Diode
S3	$i_{S_3} > 0$	$v_{S_3} < 0$	Diode

Table 1: Summary of the Proposed Semiconductors according to the catalog developed in the class
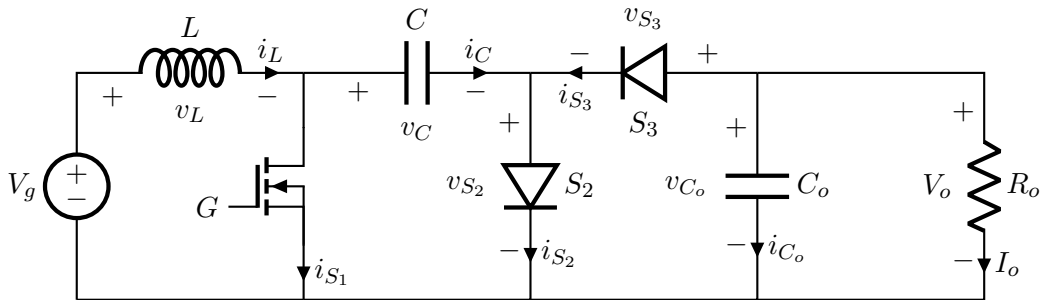

Figure 5: Final Switching Circuit with the Proposed Semiconductors: The control signal is supplied to the Gate terminal(G) of the FET.