Q1

Suitable transistor model for Q_1 : *Hybrid-*π *model*, as there is no resistor connected to the emitter terminal of the ac equivalent circuit.

Suitable transistor model for Q_2 : *T model*, as there is a resistor(R_L) connected to the emitter terminal and this will appear in series with the resistance in the emitter terminal (T model's r_e) and they can be added easily to get a single resultant resistance which makes the analysis considerably easy.

Q2

In the following figure transconductance, $g_m = I_{C_1}/V_T$, where V_T is the thermal equivalent voltage and I_{C_1} is the DC collector current of the Q_1 transistor. Moreover αi_e is the same as $\beta_2 . i_{b_2}$ where β_2 is the DC current-gain of the Q_2 transistor.

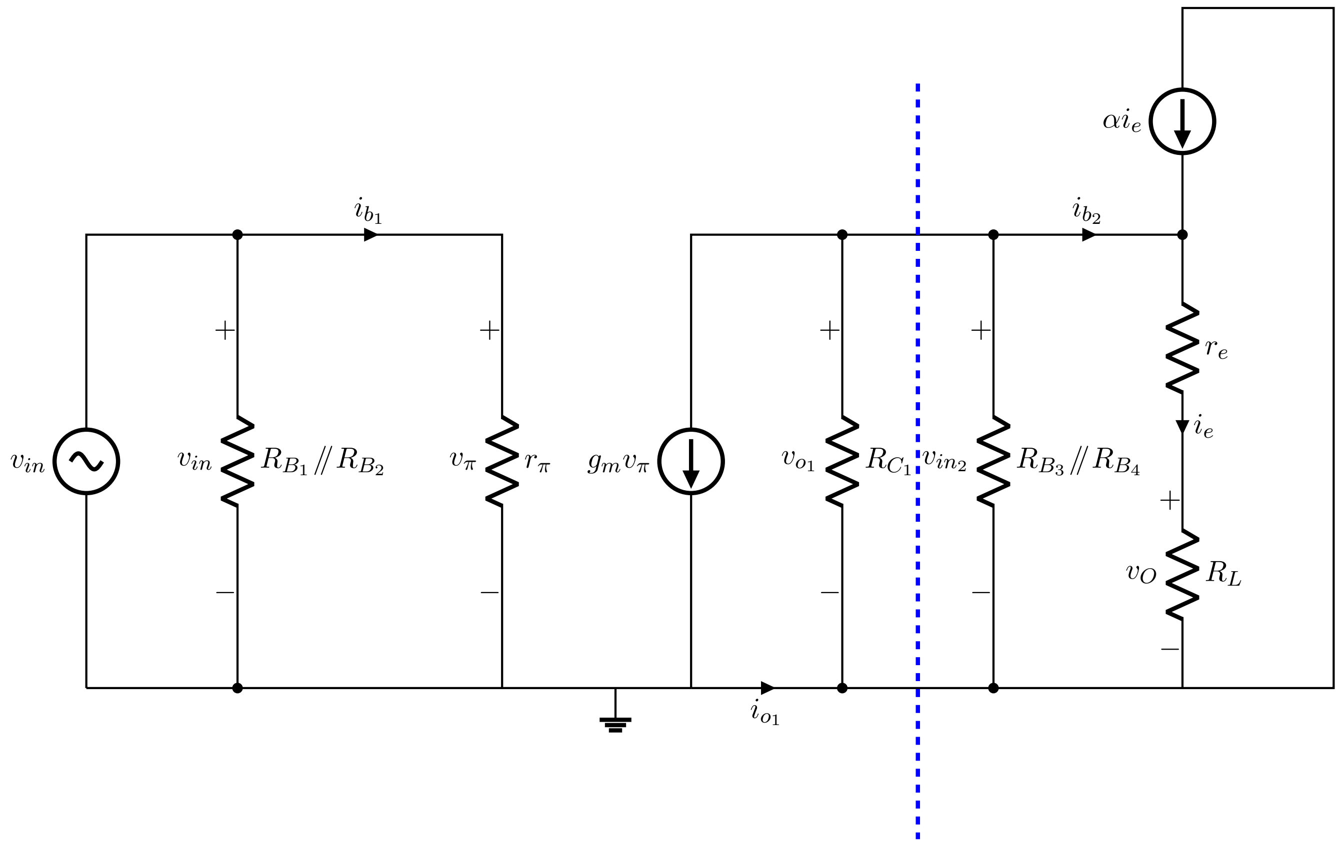

Figure 1: Small-Signal Equivalent Circuit for the given Schematic

Q3

Let the resistance seen at the base of the Q_2 be R_{ib} and the voltage at the base be v_{in_2}. Since $i_e = i_{b_2} + i_{c_2}$ which simplifies into $i_e = i_{b_2} + \beta_2 . i_{b_2} = (\beta_2 + 1) . i_{b_2} = i_e$. Therefore,

$$\begin{aligned} R_{ib} &= \frac{v_{in_2}}{i_{b_2}} \\ &= \frac{(r_e + R_L) . i_e}{i_e / (\beta_2 + 1)} \\ &= (\beta_2 + 1)(r_e + R_L) \end{aligned}$$

This R_{ib} is in parallel with the $(R_{B_3} /\!/ R_{B_4})$. Therefore the input resistance of stage 2 (R_{in_2}) can be written as follows.

$$\begin{aligned} R_{in_2} &= (R_{B_3} /\!/ R_{B_4}) /\!/ R_{ib} \\ &= (R_{B_3} /\!/ R_{B_4}) /\!/ [(\beta_2 + 1)(r_e + R_L)] \end{aligned} \tag{1}$$

Q4

Let the voltage gain of stage 2 of the amplifier be $\frac{v_O}{v_{in_2}}$, then by substituting $v_O = v_{in_2}.\frac{R_L}{r_e + R_L}$ (obtained through voltage dividing),

$$\begin{aligned} \frac{v_O}{v_{in_2}} &= \frac{v_{in_2}.\frac{R_L}{r_e+R_L}}{v_{in_2}} \\ &= \frac{R_L}{r_e + R_L} \end{aligned} \tag{2}$$

Q5

Stage 2 act as an external load in the point of view of the stage 1 and the related resistance is given by the Eq.(1). This make the total output resistance(say R_{o_1}) of the stage 1 to be as follows.

$$R_{o_1} = R_{C_1} /\!/ R_{in_2}$$

Therefore output voltage v_{o_1} of the stage 1 can be written as follows. Minus sign indicates that the voltage drop is measured in the opposite direction as illustrated in the figure, rather than the actual direction of the voltage drop. Moreover it implies the 180 degree phase shift of the output signal of the stage 1 with respect to the input signal.

$$\begin{aligned} v_{in_2} = v_{o_1} &= -i_{o_1}.R_{o_1} \\ &= -g_m.v_\pi.R_{o_1} \\ &= -g_m.v_\pi.(R_{C_1} /\!/ R_{in_2}) \end{aligned}$$

Since the v_{in} has zero internal resistance $v_{in} = v_\pi$. Then the above expression can be rearranged as follows to get the voltage gain of stage 1 of the amplifier.

$$\begin{aligned} v_{in_2} &= -g_m.v_\pi.(R_{C_1} /\!/ R_{in_2}) \\ &= -g_m.v_{in}.(R_{C_1} /\!/ R_{in_2}) \\ \frac{v_{in_2}}{v_{in}} &= -g_m.(R_{C_1} /\!/ R_{in_2}) \end{aligned} \tag{3}$$

Q6

Let the overall gain of the circuit be $A_v = v_O/v_{in}$. This overall gain of the system can be obtained by multiplying voltage gains of the two stages which we derived previously. Therefore, by multiplying the Eq.(2) with the Eq.(3) we can get the following expression for the A_v.

$$\begin{aligned} A_v &= \frac{v_O}{v_{in}} \\ &= \frac{v_O}{v_{in_2}}.\frac{v_{in_2}}{v_{in}} \\ &= \left[\frac{R_L}{r_e + R_L}\right].[-g_m.(R_{C_1} /\!/ R_{in_2})] \\ &= -\frac{R_L}{r_e + R_L}.g_m.(R_{C_1} /\!/ R_{in_2}) \\ &= -\frac{R_L}{r_e + R_L}.g_m.\{R_{C_1} /\!/ [(R_{B_3} /\!/ R_{B_4}) /\!/ ((\beta_2 + 1)(r_e + R_L))]\} \qquad (from\ Q3) \end{aligned}$$